ABSTRACT OF THE DISCLOSURE

This patent describes a boundary scan system where memories, i.e. flip flops or latches, used in data scan cells are also used functionally, but memories used in control scan cells are dedicated for test and not used functionally. The control scan cells can be scanned while the circuit is in functional mode, since their memories are dedicated. However, the data scan cells can only be scanned after the circuit transitions into test mode, since their memories are shared. This boundary scan system advantageously provides; (1) lower test circuitry overhead since the data scan cells use shared memories, (2) safe entry into test mode since the control scan cells can be scanned during functional mode to pre-load safe control conditions, and (3) avoidance of floating (i.e. 3-state) busses that can cause high current situations.